AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended) The ~~device~~ semiconductor chip of claim [[1]]9 wherein the first programmable frequency scaling circuit is a first programmable divider and the second programmable frequency scaling circuit is a second programmable divider.

4. (Currently Amended) The ~~device~~ semiconductor chip of claim 3 wherein the first programmable divider is a first programmable counter and the second programmable divider is a second programmable counter.

5. (Currently Amended) The ~~device~~ semiconductor chip of claim 3 additionally comprising control logic providing control signals to the first programmable divider and the second programmable divider.

6. (Currently Amended) The semiconductor chip of claim 5 wherein the control logic provides to the first programmable divider[[,]] a control signal controlling the loading of a programmed divider value[[,]] when the control logic detects an end of a period of the first clock.

7. (Currently Amended) The ~~device~~ semiconductor chip of claim 6 wherein the first programmable divider stores a programmable divider value and upon loading a new programmed divider value in the first programmable divider, the control logic generates an enable control signal to the first programmable divider causing the first programmable divider to hold its output until the second clock reaches a transition.

8. (Currently Amended) The ~~device~~ semiconductor chip of claim 3 wherein the phase locked loop additionally comprises a third programmable divider.

9. (Currently Amended) A semiconductor chip comprising a clock generation circuit, the clock generation circuit comprising:

a) a phase locked loop having an output;

b) a first programmable frequency scaling circuit having an input and an output, the input being coupled to the output of the phase locked loop, and the output of the first programmable frequency scaling circuit providing a first clock signal;

c) a second programmable frequency scaling circuit having an input and an output, the input being coupled to the output of the phase locked loop, and the output of the second programmable frequency scaling circuit supplying a second clock signal; and

d) ~~The device of claim 1 wherein the device comprises a semiconductor chip and the semiconductor chip additionally comprises~~ at least one control register, said at least one control register having a field ~~with fields~~ specifying ~~the~~ a scale factor of the first frequency scaling circuit and a field specifying a scale factor of the second frequency scaling circuit.

10. (Cancelled)

11. (Currently Amended) A method of operating a data processing chip, the method comprising:

a) providing a reference clock;

b) specifying a first frequency ratio between a first clock and the reference clock;

c) deriving the first clock from the reference clock with the first frequency ratio;

d) specifying a second frequency ratio between a second clock and the reference clock, the second frequency ratio specified independent of the first frequency ratio;

e) deriving the second clock from the reference clock with the second frequency ratio;

f) clocking first circuitry with the first clock and clocking second circuitry with the second clock; and

g) ~~The method of operating a data processing chip of claim 10 additionally comprising~~ changing the frequency of the first clock on the fly.

12. (Currently Amended) A method of operating a data processing chip, the method comprising:

a) providing a reference clock;

b) specifying a first frequency ratio between a first clock and the reference clock;

c) deriving the first clock from the reference clock with the first frequency ratio;

d) specifying a second frequency ratio between a second clock and the reference clock, the second frequency ratio specified independent of the first frequency ratio;

e) deriving the second clock from the reference clock with the second frequency ratio;

f) clocking first circuitry with the first clock and clocking second circuitry with the second clock; and

g) ~~The method of operating a data processing chip of claim 10 additionally comprising~~ placing the data processing chip in a first power saving mode by changing the first frequency ratio such that the first circuitry is clocked at a lower rate.

13. (Previously presented) The method of operating a data processing chip of claim 12 additionally comprising placing the data processing chip in a second power saving mode by reducing the frequency of the reference clock.

14. (Previously presented) The method of operating a data processing chip of claim 12 wherein the data processing chip processes data in a mobile telephone and placing the data processing chip in a first power saving mode occurs while a call is in process on the mobile telephone.

15. (Previously presented) The method of operating a data processing chip of claim 13 wherein the data processing chip is inside a mobile telephone and placing the data processing chip in a second power saving mode occurs while the mobile telephone is not in use to make a call.

16. (Currently Amended) The method of operating a data processing chip of claim ~~10~~ 11 additionally comprising placing the data processing chip in a first power saving mode by changing the first frequency ratio such that the first circuitry is clocked at a lower rate without changing the frequency of the reference clock or the second clock.

17. (Currently Amended) The method of operating a data processing chip of claim ~~10~~ 11 wherein the frequency of the first clock and the frequency of the second clock are not integer multiples of each other.

18. (Currently Amended) The method of operating a data processing chip of claim ~~10~~ 11 wherein the data processing chip comprises at least one control register with a field ~~fields~~ specifying ~~the~~ a frequency ratio between the reference clock and the first clock and a field specifying a frequency ratio between the reference clock and the second clock.

19. (Previously presented) A method of operating a data processing chip having first circuitry and circuitry that interfaces to devices external to the first circuitry wherein the first circuitry is clocked with a first clock and the circuitry that interfaces to devices external to the first circuitry is clocked with a second clock, the frequency of the first clock and the second clock being controllable, the method comprising:

a) loading a control location with a first value that controls the frequency of the first clock;

b) loading a control location with a second control value that controls the frequency of the second clock;

c) providing a new value for at least one of the first clock and the second clock;

d) waiting until a defined time relative to the period of the second clock while holding the state of the first clock; and

e) loading the new value in a control location at the defined time.

20. (Original) The method of claim 19 wherein the second clock operates at a slower frequency than the first clock.

21. (Original) The method of claim 20 wherein the data processing chip processes data in a mobile telephone and providing a new value for one of the first clock and the second clock comprises providing a new value for the first clock while a call is in process on the mobile telephone.

22. (Original) The method of claim 19 wherein providing the new value for one of the first clock and the second clock comprises setting a value in a control register.

23. (Previously presented) The method of claim 22 wherein loading a control location comprises loading a programmable counter.

24. (Previously presented) The method of claim 19 wherein the act c) of providing a new value comprises providing a new value for the first clock to place a battery operated electronic device in a power saving mode.

25. (Previously presented) The method of claim 24 additionally comprising replacing the new value stored in the control location with the first value to take the electronic device out of power saving mode.

26. (New) The method of operating a data processing chip of claim 12 wherein the frequency of the first clock and the frequency of the second clock are not integer multiples of each other.

27. (New) The method of operating a data processing chip of claim 12 wherein the data processing chip comprises at least one control register with a field specifying a scale factor of the first frequency scaling circuit and a field specifying a scale factor of the second frequency scaling circuit.

28. (New) The semiconductor chip of claim 9 further comprising:

a) internal circuitry clocked by the first clock signal; and

b) at least one interface circuit clocked by the second clock signal, the interface circuit adapted to interface to external circuitry.

29. (New) The method of claim 11 wherein clocking the first circuitry with the first clock and clocking the second circuitry with the second clock comprises clocking circuitry internal to the data processing chip with the first clock and clocking circuitry interfacing to circuitry external to the data processing chip with the second clock.

30. (New) The method of claim 12 wherein clocking the first circuitry with the first clock and clocking the second circuitry with the second clock comprises clocking circuitry internal to the data processing chip with the first clock and clocking circuitry interfacing to circuitry external to the data processing chip with the second clock.